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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,477	01/28/2004	Leonard Forbes	M4065.0381/P381-A	9433

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

MAIL DATE	DELIVERY MODE
06/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/765,477	FORBES ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *68-102* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *89* is/are allowed.

6)☒ Claim(s) *68,90,91,94,98 and 100* is/are rejected.

7)☒ Claim(s) *69-88, 92-93, 95-97, 99, 101-102* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amendment mailed on 09 March 2007.

2. Currently, claims 68-102 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 68, 90-91, 94, 98, and 100 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu (US 6,312,995 B1).

Regarding claim 68 and 94

Yu discloses a method of forming a semiconductor transistor (figs. 1, 2a-2e and accompanying text). The method comprises: forming a first gate dielectric 112 over a substrate 110 (fig. 2a and col. 3, lines 58-62); forming a first conductive gate region 114 over the first gate dielectric (fig. 2a and col. 3, line 62 - col. 4, line 3); forming a dielectric layer 117 on the sides of the first conductive layer (fig. 2a and col. 4, lines 8-10); forming a second gate dielectric

117 over the substrate (fig. 112)[1]; forming a second conductive gate region 124 over the second gate dielectric, adjacent to the dielectric layer 117, and on the sides of the first conductive region (fig. 2d and col. 4, lines 35-52); and forming source and drain regions 120 in the substrate to define a channel region between them and beneath the first and second conductive gate regions (fig. 2d and col. 4, lines 19-22), wherein all portions of the first gate dielectric, first conductive gate region, second gate dielectric, and second conductive gate region are wholly between the source and drain regions. The second conductive region is capable of forming at least one of virtual source ad drain regions when receiving a bias voltage (col. 3, lines 45-52).

Regarding claims 90 and 91

Again, Yu discloses a method of forming a semiconductor transistor (figs. 2a-2e and accompanying text). The method comprises: providing a substrate 110 (fig. 2a); forming a first gate dielectric layer 112 over the substrate (fig. 2a); forming a first gate electrode 114 having sidewalls over the first gate dielectric layer (fig. 2a), wherein the first gate electrode has a first work function (fig. 1 and col. 3, lines 7-11); forming a dielectric layer 117 on the sidewalls of the first gate electrode (fig. 2a); forming a second gate dielectric layer 112 over the substrate (fig. 2c, see Footnote No. 1); forming a pair of second gate electrodes 124 over the second gate dielectric layer and adjacent to the dielectric layer 117, the second gate electrodes being separated from the first gate electrode by

[1] The second gate dielectric layer is that portion of the dielectric layer 112 not covered by the

the dielectric layer (fig. 2d), wherein the pair of second gate electrodes has a second work function which is different than the first work function (fig. 1 and col. 3, lines 7-11); forming a conductive cap 128 over each of the gate electrodes (fig. 2e and col. 5, lines 1-4); forming insulating sidewalls 118 adjacent to the conductive cap and the gate electrodes (fig. 2e and col. 4, lines 18-22), and forming source and drain regions 120 in the substrate to define a channel region between them and beneath the first and second conductive type gate regions (fig. 2d), wherein all portions of the first gate dielectric, first gate electrode, second gate dielectric layer, and pair of second gate electrodes are wholly between the source and drain regions.

The second work function is more negative than the first work function (col. 3, lines 11-24).

The pair of second gate electrodes is capable of forming respective virtual source and drain regions when receiving a bias voltage (col. 3, lines 45-52).

Regarding Claim 100

Yu discloses a method of forming a semiconductor transistor, comprising: forming source and drain regions 20, 22 defining a channel region therebetween (fig. 2B and col. 4, lines 19-22); and forming first and second gate regions 124a, 124b capable of being independently biased (fig. 2D and col. 4, lines 35-52), the second gate region forming at least one of virtual source and drain regions when receiving bias voltage (col. 3, lines 45-52).

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gate region.

Allowable Subject Matter

4. Claims 69-88, 92-93, 95-97, 99, 101-102 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 89 is allowable over the prior art of record.

Response to Arguments

5. Applicant's arguments filed on 09 March 2007 have been fully considered but they are not persuasive.

Applicant argues that Yu does not teach that all portions of said first gate dielectric, first conductive gate region, second gate dielectric, and second conductive gate region are wholly between said source and drain regions. Figure 2 of Applicant's disclosure shows overlapping of the second conductive gate regions 42a, 42b with source/drain extensions 46, which form part of the source and drain regions 32. Therefore, bases on Applicant's disclosure, the term "wholly between" does not preclude overlapping of the source and drain regions.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TMT
11 June 2007

Mary Wilczewski
Primary Examiner